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Fabrication of Co/Si nanowires by ultrahigh-vacuum scanning tunneling microscopy on hydrogen-passivated Si(100) surfaces

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We have fabricated nanometer width Co/Si metal lines on Si(100) surfaces by ultrahigh-vacuum scanning tunneling microscopy (UHVSTM) based nanolithography on the hydrogen-passivated surface, combined with vapor deposition of Co at room temperature and subsequent annealing. The STM tip was used to define depassivated lines (<10 nm in width) by electron stimulated hydrogen desorption, and subsequently Co was deposited at a submonolayer coverage. Annealing of the substrate at 410 °C (just below hydrogen desorption) improves the structure of the wire due to silicidation, whereas the as-deposited wire is very granular (comparable to other materials in previous studies). © *1999 American Institute of Physics.* [S0021-8979(99)02202-1]

I. INTRODUCTION

Scanning tunneling and atomic force microscopy (STM and AFM) have been proven to be unique tools for the *controlled* fabrication of nanoscale *structures*.[1,2] For example, the local field of a STM tip or a conductive AFM tip has been used to oxidize locally a sample area which was then used as mask for selective etching.[1] In other cases, ultrahigh-vacuum (UHV) STM was used to selectively desorb hydrogen from Si with atomic scale precision opening the possibility to pattern areas of various shapes and sizes.[2] Metallization proceeds by means of chemical or physical vapor deposition (CVD, PVD) techniques[2–4] of metal adatoms which nucleate selectively on small depassivated areas due to the increased density of reaction sites. It is hoped that such small metal patterns can be used as model systems to study aspects of nanoscale electronics such as single-electron tunneling.[1,2] While this procedure leaves isolated islands around the pattern, these clusters do not form a continuous film and thus are not expected to pose a severe problem in electronic transport experiments. Even if electron hopping between the isolated islands were possible, charging effects would supress any conductivity.

Metallization techniques have been demonstrated recently for Fe and Al, producing nanowire structures fabricated by CVD and PVD.[2–4] These structures were strongly granular in structure and apparently could not be improved by temperature treatment. Besides the fabrication of pure metal structures (like Al and Cu metallization in ultra large scale integrated (ULSC) devices), *silicides* are very promising candidates for the fabrication of metallic nanowires. Co merits special attention since it forms silicides with characteristic properties like low electrical resistivity, and small lattice mismatch with the Si substrate at room temperature (RT),[5–7] which led to its widespread application in microelectronics (e.g., gates and contacts). Co also has the advantage that all its silicide phases are metallic.[8] The formation temperature of $CoSi_2$ at 648–773 K (Refs. 5, 9) in solid phase epitaxy, should make it possible to achieve site selective silicide formation below the H desorbtion temperature of 734 K.[10]

A RT nucleation study of Co deposited onto H wet-passivated Si(111) surfaces[11] showed that Co nucleates in sparse nonepitaxial islands. Similar behavior was also observed for Co on hydrogen-passivated Si(100) surfaces (H-Si(100)) prepared in UHV and studied *in situ* by STM.[12] This behavior is quite different from the behavior of submonolayer growth of Co on bare Si(100) where the missing passivation layer allows interstitial diffusion and the reaction of Co with the Si substrate.[7] However, selective nucleation of Co adatoms on locally depassivated H-Si(100) surfaces for nanoscale metallization still remains unexplored. This and the annealing behavior of such structures will be the topic of the present article, where our focus will be primarily on the fabrication of nanoscale Co/Si wires with width less than 10 nm.

II. EXPERIMENTAL PROCEDURE

P-doped Si(100) samples of resistivity 30 Ω cm were cleaned by resistive heating (lengthy degassing up to 750 °C and flashing to 1200 °C) in an UHV chamber of base pressure $\sim 1\times10^{-10}$ mbar, to form Si(100) 2×1 clean reconstructed surfaces. Sample temperature was determined by pyrometry to better than ±10 °C above 400 °C. The Si samples were dosed with atomic H from high purity H_2 which was dissociated by a hot (~1500 °C) *W* filament. The passivation lasted 6 min at a pressure 3×10^{-6} mbar yielding a dose of ~1000 L (1 L$=10^{-6}$ Torr s), with the sample held at ~400 °C to ensure monohydride termination.[2,4] Co was e-beam evaporated at a rate ~0.0017 nm/s (which was calibrated by a quartz crystal microbalance to within

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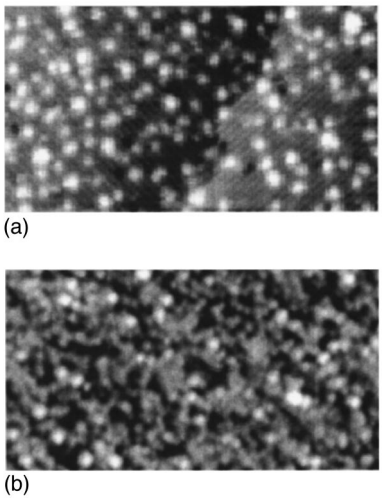

FIG. 1. Filled state images (bias -2 V and current 0.12 nA, scan size 40 $\times 22$ nm) of 0.2 ML of Co deposited at RT on (a) H-Si(100) surface, and (b) on bare Si(100)2×1 surface.

$\sim$10% error), while the pressure did not exceeded $\leqslant 3\times10^{-9}$ mbar. The samples were imaged and patterned *in situ* in a STM chamber held at a pressure $\sim 1.5\times10^{-10}$ mbar. For the STM mechanically cut PtIr tips were used.

III. RESULTS—DISCUSSION

Upon submonolayer deposition of Co on a H-Si(100) 2×1 surface at RT, the H passivation layer stays intact and blocks the reaction with the Si substrate. Figure 1(a) shows the formation of Co clusters on such a surface. While for deposition on the bare Si(100) 2×1 surface the absence of H allows the interstitial diffusion of Co atoms into the Si,[7] accompanied by the first silicidation reaction. The result of such a reaction process is depicted in Fig. 1(b). In comparison, Al forms a well ordered dimer-row structure on bare Si(100) for coverage below 0.5 monolayers (ML; 1 ML $=6.8\times10^{14}$ atoms/cm^2).[4,13]

Figure 2(a) illustrates the ability of a mechanically cut STM tip to form patterns on a H-Si(100) surface by electron stimulated H desorption. Depassivated lines about 8 nm wide were written with current $I_t=5$ nA, sample bias $V_b=7$ V, and a writing speed of 300 nm/s. Under these patterning conditions ($|V_b|>6$ V), H desorbs according to the Si–H bonding–antibonding transition mechanism.[2] The lines appear higher than the rest of the H-Si(100) surface due to the increased density of states (from the H-free Si dangling bonds) for tunneling.[2] Figure 2(b) shows the possibility with the mechanically cut tips to define depassivated lines of one to two dimer rows wide[14] opening the possibility for the fabrication of atomic wires.

Figures 3 and 4 depict Co/Si lines on a H-Si(100) sample after deposition of 0.13 ML of Co at RT. The depassivated lines were written in a manner similar to that of Fig. 2(a) at a length of $\sim$2400 nm. A dense concentration of Co in the

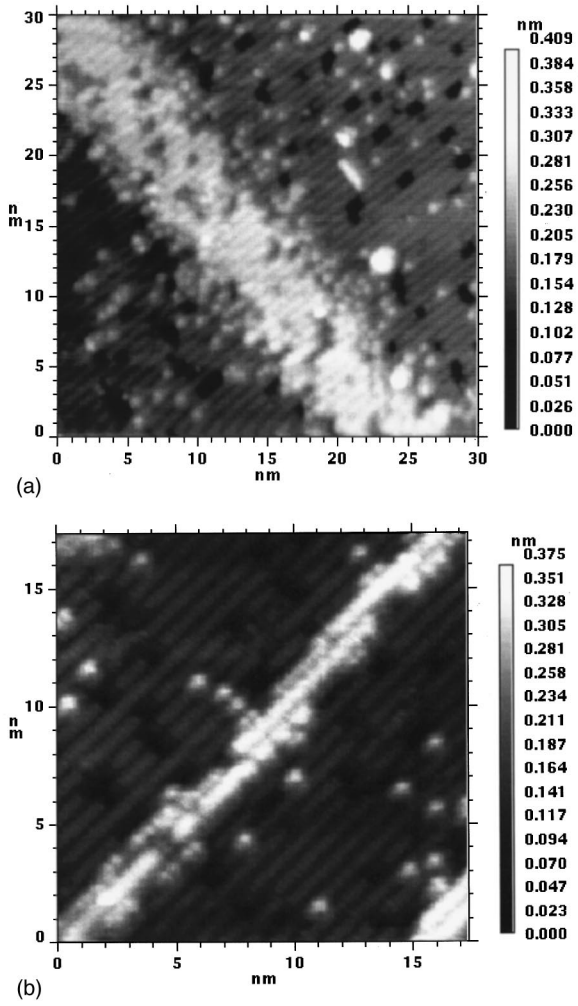

FIG. 2. (a) Depassivated line on a H-Si(100) surface created with STM at a writing speed 300 nm/s, current 5 nA, and bias voltage 7 V. Filled state image acquired with bias -2 V and current 0.12 nA. The patterned line has a width approximately 8 nm. (b) Line created with a writing speed 100 nm/s, current 3 nA, and bias voltage 5.5 V. Filled state image acquired with bias -1.67 V and current 0.48 nA.

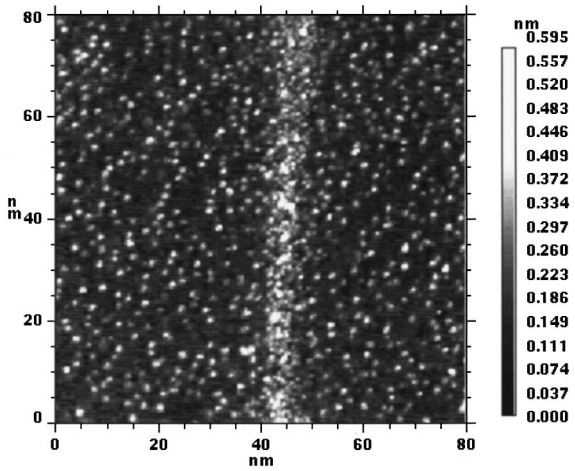

FIG. 3. 0.13 ML of Co deposited at RT resulting in wire (wire patterning parameters as in Fig. 2(a) width approximately 8–9 nm. Filled state image acquired with bias -2 V and current 0.12 nA.

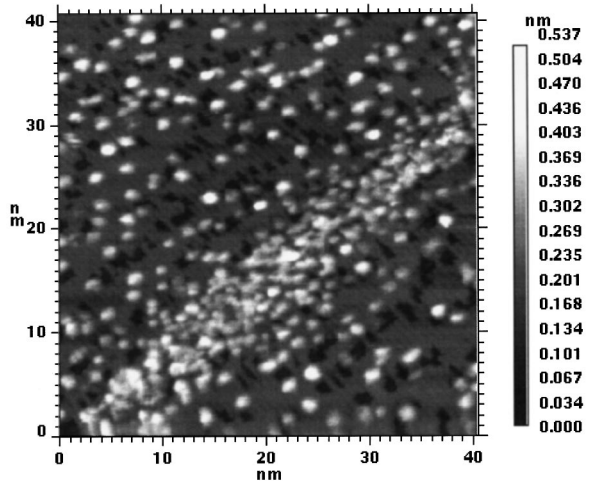

FIG. 4. Details of the RT Co/Si wire of Fig. 3. Filled state image acquired with substrate bias −1.82 V and current 0.48 nA.

depassivated lines occurs with respect to the monohydride areas. Co atoms nucleate randomly even rather close to the wire at distances 3–5 nm which are comparable with the island spacing on the monohydride side.

We do not observe a significant depletion zone around the wire boundary, which may be different for the case of PVD of Al.[4] This is surprising since one expects, due to the high reactivity of the depassivated sites a sticking coefficient close to one. One reason might be that the mean free path for surface diffusion of Co is significantly longer on the H-Si(100) than the mean spacing of the Co clusters[15] which would camouflage the reduction of Co around the wire. Another reason could be that the sticking coefficient of the depassivated area reduces with the amount of deposited material. This would be expected since the number of unreacted Si sites reduces with progressing deposition.

The RT wire structure is rather granular which can be attributed to limited silicidation at RT. The wire width is approximately 8–9 nm which is comparable to the depassivated line width [Fig. 1(a)], indicating significant control over lateral feature size. In comparison with former metallization studies, the Co/Si wires appear more compact. While they have better defined boundaries than Fe wires formed by CVD of $Fe(CO)_5$.[3] the boundaries appear more irregular than those formed in Al PVD.[4]

Device fabrication processing at elevated temperature is often unavoidable. Some metals suffer under high temperature treatments from the dissolution in Si (e.g., Al/Si structures degrade upon annealing >400 °C),[9] while other metals form upon annealing stable silicides. Co has the advantage that all its silicide phases are metallic[8] while, for example, $FeSi_2$ is usually semiconducting (depending on the corresponding phase).[16]

Figure 5 shows a sample where 0.13 ML of Co was deposited at RT on a H-Si(100) surface with depassivated lines of about ~4–5 nm wide (patterned with $I_t=2$ nA, $V_b=7$ V, and writing speed 300 nm/s) after which the surface was annealed at 410 °C for 20 s. The progressing silicidation reaction in the wire area leads to an increase in silicide volume which leads to a more distinct and compact structure

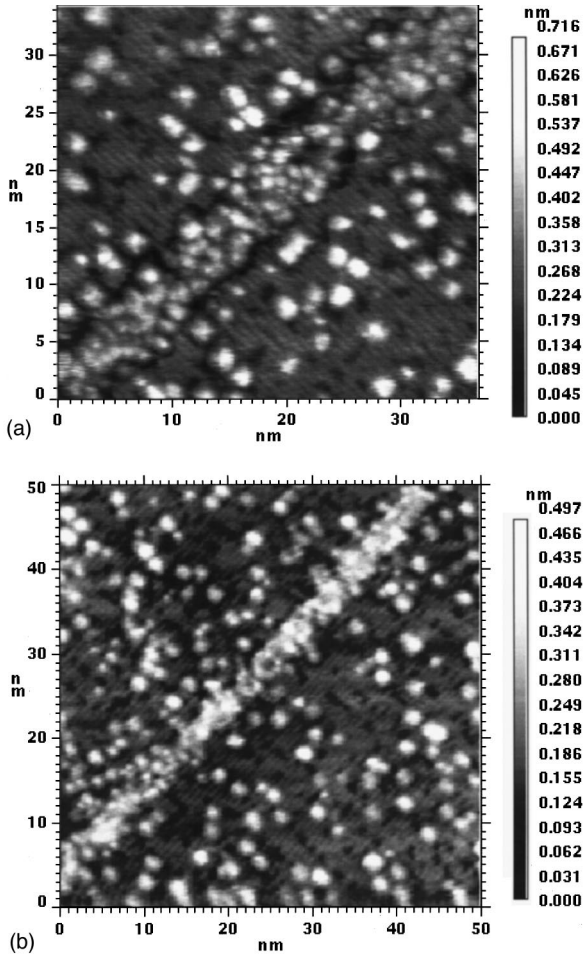

FIG. 5. Co/Si wire deposited at RT and annealed at 410 °C for 20 s. (a) Wire perpendicular to dimer rows (filled state image acquired with bias voltage −1.69 V and current 0.34 nA). (b) Wire along the dimer rows (filled state image acquired with bias voltage −1.89 V and current 0.28 nA).

than that formed at RT. The monohydride side remains intact even closely to the wire boundary (which appears sharper than that at RT) despite the annealing processes since H starts to desorb at higher temperatures ($\leqslant$470 °C).[10]

Notably, differences appear when the wire is formed perpendicular [Fig. 5(a)] and along the dimer rows [Fig. 5(b)]. In the second case a more compact structure with more regular boundaries is found. This finding is in good agreement with the shape and appearance of $CoSi_2$ islands on Si(100) formed at elevated temperature[7] which show edges which are straight on the atomic scale parallel to the dimer rows while they can be rather rough in the perpendicular direction. Possible reasons might be the different directional surface strain and adatom mobility parallel and perpendicular to the Si dimer rows (details will be given elsewhere[14]). The difference in linewidth in Figs. 5(a) and 5(b) is attributed to slightly different linewidths defined by the STM tip during patterning on the H-Si(100) surface.

From our earlier studies we have learned that the convolution with the tip geometry leads to an exaggerated apparent lateral size of Co clusters on H-Si(100) surfaces.[12] We therefore choose for a study in the submonolayer regime. From the present study we can conclude that 0.2–0.4 ML of Co

should be sufficient for the formation of a closed metallic wire. The necessary amount of Co might even be reduced by deposition at elevated substrate temperature[12] which would lead to an increased material transport to the depassivated areas. For closing of the film on the H-passivated area coverages in the ML regime (3–6 ML) are expected (see also Ref. 11).

IV. CONCLUSIONS

In conclusion, we illustrated the applicability of Co for nanoscale metallization by means of STM nanofabrication and PVD. Due to its strong reaction with the Si, leading to silicide formation, Co stands as a potentially suitable candidate for the fabrication of nanostructures on Si. Experiments are now in progress to create metallic nanostructures connected to macroscopic contacts that will allow further characterization of such structures by electrical transport measurements addressing, therefore, important issues in integrated circuit technology.

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